What is Claimed is:

1. A method of fabricating a bipolar semiconductor device from a structure, the structure comprising:

a substrate;

a semiconductor subcollector layer overlying the substrate;

a semiconductor collector layer overlying the semiconductor subcollector contact layer;

a semiconductor graded base-collector layer overlying the semiconductor collector layer;

a semiconductor base layer overlying the semiconductor graded base-collector layer;

a semiconductor graded emitter-base layer overlying the semiconductor base layer;

a semiconductor emitter overlying a first portion of the semiconductor graded emitter-base layer;

at least one base contact pad overlying a second portion of the semiconductor graded emitter-base layer;

an emitter contact pad overlying the semiconductor emitter having a height; and

at least one collector contact pad overlying at least one of the semiconductor sub collector layer and the semiconductor collector layer, wherein the method comprises the steps of:

forming at least one collector contact post and at least one base contact post, the at least one collector contact post overlying the at least one collector contact pad and the at least base contact post overlying the at least one base contact pad, the at least one collector contact post and the at least one base contact post substantially reaching the emitter contact pad height;

forming a passivation layer to encapsulate the structure, the at least one collector contact post, and the at least one base contact post;

curing the passivation layer; and

exposing the at least one collector contact post, the at least one base contact post, and the emitter contact pad through the cured passivation layer to form the bipolar semiconductor device.

2. A method of claim 1, further comprising the step of substantially planarizing the passivation layer, the step of substantially planarizing the passivation layer comprising the steps of the forming a passivation layer and the curing of the passivation layer.

3. The method of claim 1, wherein the step of forming at least one collector contact post and at least one base contact post comprises a lift-off step.

4. The method of claim 1, wherein at least one of the at least one collector contact post and the at least one base contact post comprises Pt, Au and Ti.

5. The method of claim 1, wherein the step of forming a passivation layer comprises spinning on benzocyclobutene ("BCB").

6. The method of claim 1, wherein the step of curing the passivation layer comprises the step of heating the passivation layer in an N_2 atmosphere to a temperature substantially in the range of 250-350°C for a period substantially in the range of 1-30 minutes.

7. The method of claim 1, wherein the step of exposing the at least one collector contact post, the at least one base contact post, and the emitter contact pad through the cured passivation layer comprises the step of etching the cured passivation layer.

8. The method of claim 7, wherein the step of etching the cured passivation layer further comprises the step of detecting an endpoint to the etching of the planarized cured passivation layer.

9. The method of claim 7, wherein the step of etching the cured passivation layer comprises a Reactive Ion Etching step.

10. The method of claim 7, wherein the step of etching employs a chemistry of at least one of CF_4:O_2 at an approximate ratio of 40:60 and SF_6:O_2 at an approximate ratio of 6:10.

11. A method of fabricating a III-V heterojunction bipolar semiconductor device from a structure, the structure having a height and comprising:

an InP substrate;

an n+ InGaAs subcollector overlying the substrate;

an n- InP collector overlying the subcollector;

a first graded quaternary InGaAsP base-collector layer overlying the collector;

an InGaAs base overlying the first graded quaternary layer;

a second graded quaternary InGaAsP emitter-base layer overlying the base;

an n- InP emitter overlying a first portion of the second graded quaternary layer;

at least one base contact pad overlying a second portion of the second graded quaternary layer, the base contact comprising at least one of Pd, Pt and Au and having a base contact pad height;

an n+ InGaAs emitter contact pad overlying the emitter and having an emitter contact pad height; and

at least one collector contact pad overlying at least one of the subcollector and the collector, the at least one collector contact pad substantially reaching the base contact pad height, wherein the method comprises the steps of:

forming at least one collector contact post overlying the at least one collector contact pad and at least one base contact post overlying the at least one base contact pad, the at least one collector contact post and the at least one base contact post substantially reaching the emitter contact pad height and comprising at least one of Ti, Pt and Au;

encapsulating the structure, the at least one collector post, the at least one base post and the emitter contact pad with a polymer layer having a encapsulating height of approximately twice the height of the structure;

curing the polymer layer in an N_2 atmosphere substantially in the range of 250-350°C for a time period substantially in the range of 1-30 minutes to anneal the pads, the posts, and allow the base contact pad to directly interface with the base; and

etching the cured polymer layer to expose the at least one base post, the at least one collector post and the emitter contact pad through the cured polymer layer and form the III-V heterojunction bipolar semiconductor device.

12. The method of claim 11, wherein the step of forming a collector contact post and a base contact post comprises a lift-off step.

13. The method of claim 11, wherein the polymer layer is substantially planarized by the step of encapsulating with a polymer layer step and the step of curing the polymer layer step.

14. The method of claim 11, wherein the polymer layer comprises spun on benzocyclobutene.

15. The method of claim 11, wherein the step of etching the cured polymer layer comprises a Reactive Ion Etching step and employs at least one of CF_4 at an approximate ratio of 40:60 and SF_6:O_2 at an approximate ratio of 6:10.

16. A method of fabricating a semiconductor device having a semiconductor region, the method comprising the steps of:

forming at least one conductive post overlying the semiconductor region to form a structure;

encapsulating the structure and the at least one conductive post to form a planarized cured passivation layer; and

exposing the at least one conductive post through the planarized cured passivation layer to form the semiconductor device.

17. The method of claim 16, wherein the step of forming at least one conductive post comprises a lift-off step, and the at least one conductive post comprises at least one of Pt, Au and Ti.

18. The method of claim 16, wherein the step of encapsulating the structure and the at least one conductive post comprises the steps of:

forming the passivation layer by spinning on benzocyclobutene ("BCB"); and

heating the passivation layer in an N_2 atmosphere to a temperature substantially in the range of 250-350°C for a period substantially in the range of 1-30 minutes, such that the passivation layer is spun on, cured and planarized.

19. The method of claim 16, wherein the step of exposing the at least one conductive post comprises the step of etching the planarized cured passivation layer.

20. The method of claim 19, wherein the step of etching the planarized cured passivation layer comprises a Reactive Ion Etching step and employs a chemistry of at least one of CF_4:O_2 at an approximate ratio of 40:60 and SF_6:O_2 at an approximate ratio of 6:10.